FIG. 1

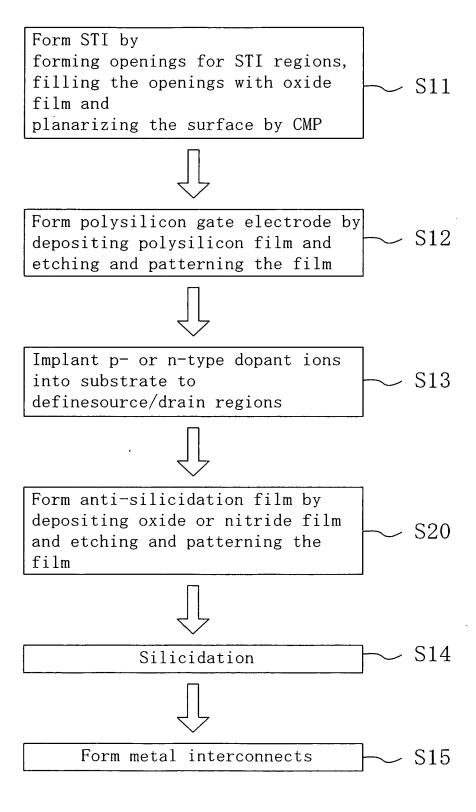


FIG. 2

<u>S20</u>

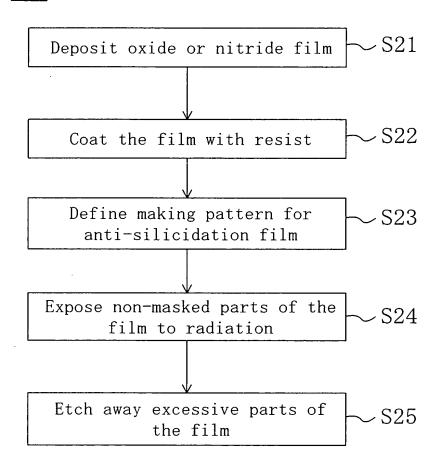


FIG. 3A 12

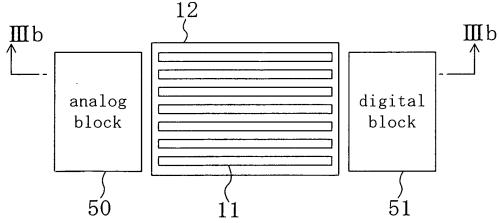


FIG. 3B

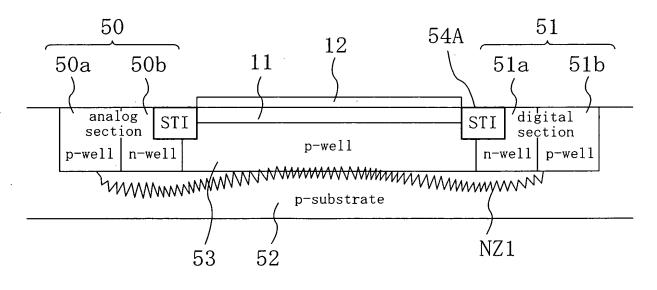


FIG. 4A

Nb

analog
block

50

TVb

digital
block

51

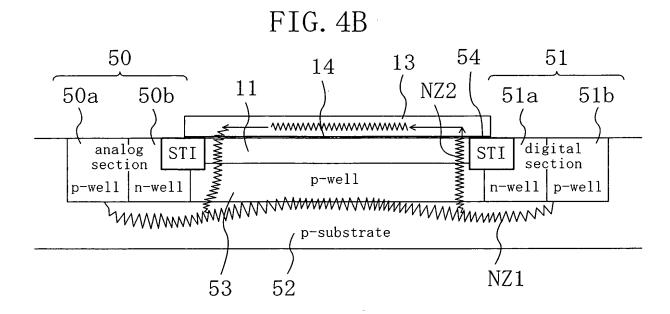


FIG. 5A

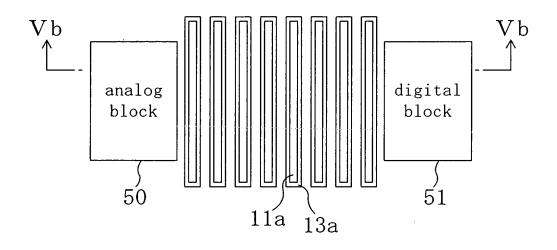
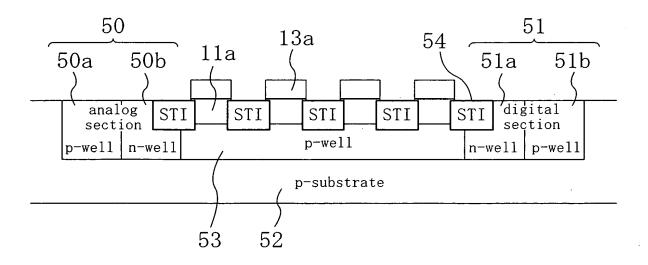
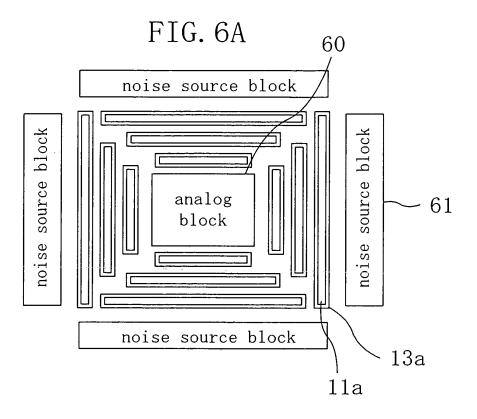


FIG. 5B





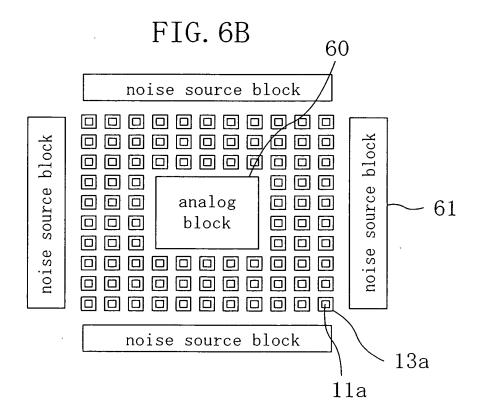


FIG. 7A

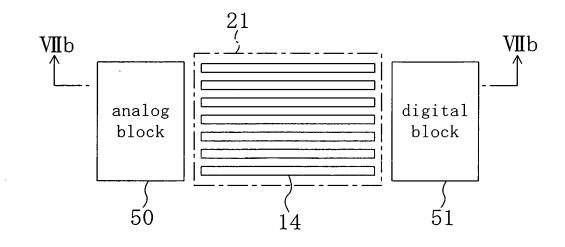


FIG. 7B

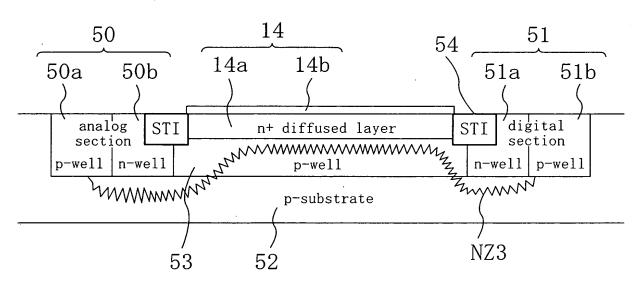


FIG. 8

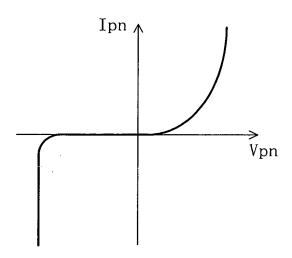


FIG. 9

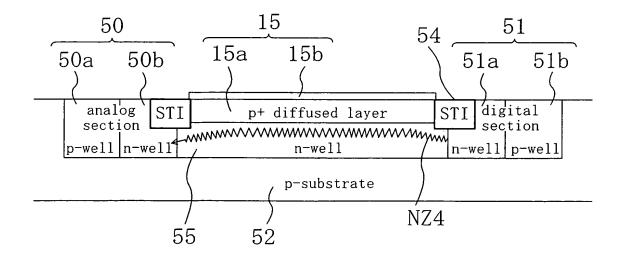


FIG. 10A

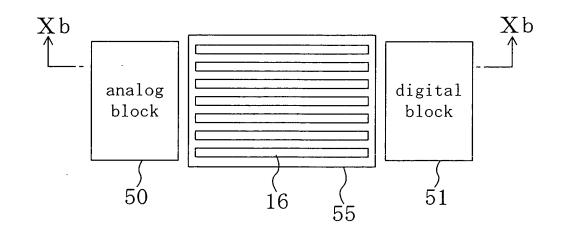


FIG. 10B

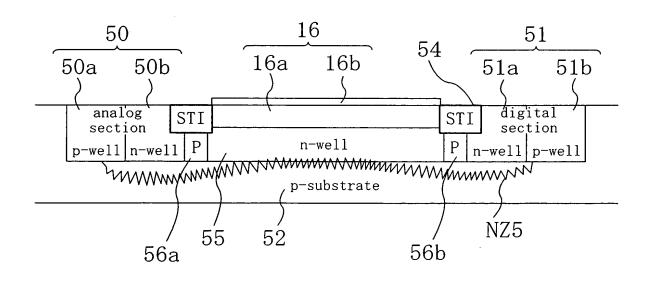


FIG. 11

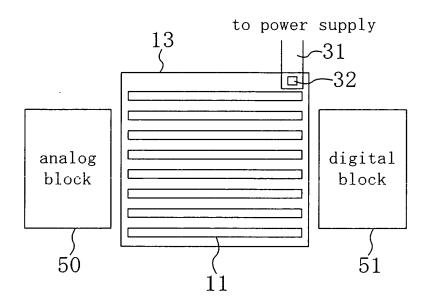


FIG. 12

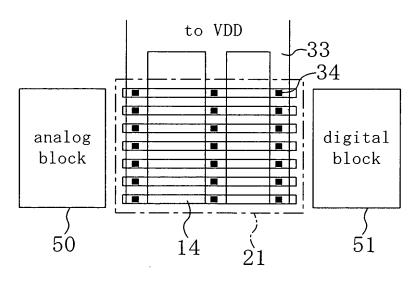


FIG. 13

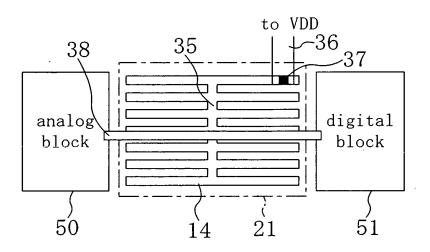


FIG. 14A

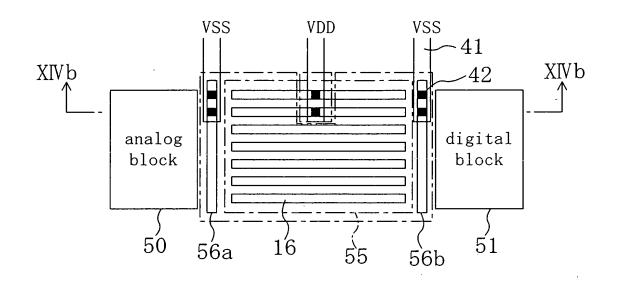


FIG. 14B

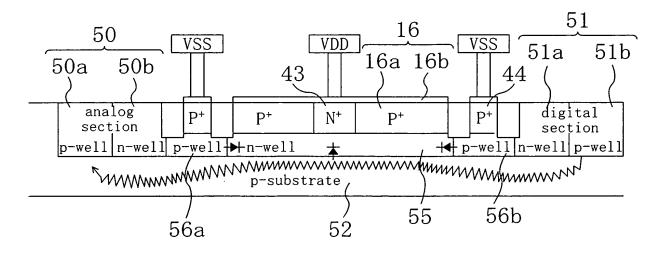
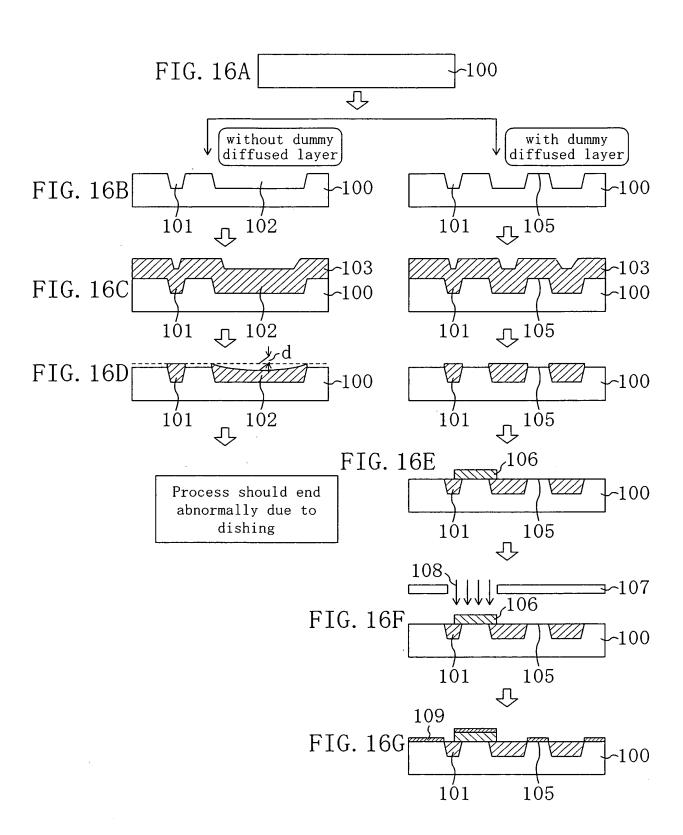


FIG. 15

Form STI by forming openings for STI regions, filling the openings with oxide film and planarizing the surface by CMP Form polysilicon gate electrode by S12 depositing polysilicon film and etching and patterning the film Implant p- or n-type dopant ions S13 into substrate to definesource/drain regions S14 Silicidation Form metal interconnects S15



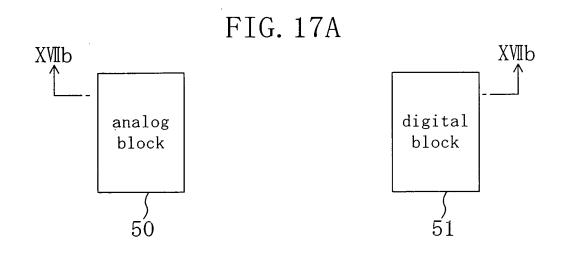


FIG. 17B

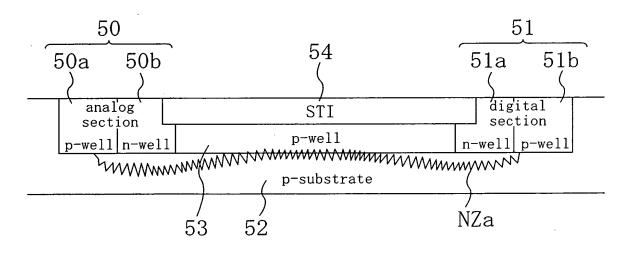


FIG. 18A

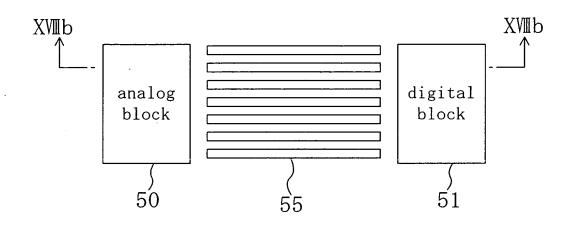


FIG. 18B

